Table of Contents

UNITED STATES
SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM 8-K

CURRENT REPORT
Pursuant to Section 13 or 15(d) of the Securities Exchange Act of 1934

Date of Report (Date of earliest event reported): October 6, 2004

PDF Solutions, Inc.

(Exact name of registrant as specified in its charter)

Delaware	**000-31311**	**25-1701361**
(State or other jurisdiction of incorporation)	(Commission File Number)	(IRS Employer Identification No.)

333 West San Carlos Street **Suite 700** **San Jose, CA**	**95110**
(Address of principal executive offices)	(Zip Code)

Registrant's telephone number, including area code: (408) 280-7900

Not Applicable
(Former name or former address, if changed since last report.)

Check the appropriate box below if the Form 8-K filing is intended to simultaneously satisfy the filing obligation of the registrant under any of the following provisions:

☐ Written communications pursuant to Rule 425 under the Securities Act (17 CFR 230.425)

☐ Soliciting material pursuant to Rule 14a-12 under the Exchange Act (17 CFR 240.14a-12)

☐ Pre-commencement communications pursuant to Rule 14d-2(b) under the Exchange Act (17 CFR 240.14d-2(b))

☐ Pre-commencement communications pursuant to Rule 13e-4(c) under the Exchange Act (17 CFR 240.13e-4(c))

TABLE OF CONTENTS

Item 7.01 Regulation FD Disclosure.
Item 9.01. Financial Statements and Exhibits.
SIGNATURE
EXHIBIT INDEX
EXHIBIT 99.1
EXHIBIT 99.2

Table of Contents

Item 7.01 Regulation FD Disclosure.

On October 6, 2004, the Registrant issued two press releases, the text of each are set forth on Exhibits 99.1 and 99.2 hereto, respectfully.

The information in this Item 7.01, including Exhibits 99.1 and 99.2, is furnished and shall not be deemed "filed" for the purposes of Section 18 of the Securities Exchange Act of 1934, as amended, or otherwise subject to the liabilities under that Section and shall not be deemed to be incorporated by reference into the filings of the Company under the Securities Act of 1933, as amended.

Item 9.01. Financial Statements and Exhibits.

(c) Exhibits

Exhibit No.	Description
99.1	Press Release issued by PDF Solutions, Inc. dated October 6, 2004.
99.2	Press Release issued by PDF Solutions, Inc. dated October 6, 2004.

Table of Contents

SIGNATURE

Pursuant to the requirements of the Securities Exchange Act of 1934, the Registrant has duly caused this report to be signed on its behalf by the undersigned hereunto duly authorized.

PDF Solutions, Inc.
(Registrant)

Date: October 6, 2004

By: /s/ P. Steven Melman
P. Steven Melman
Vice President, Finance and Administration and Chief Financial Officer

Table of Contents

EXHIBIT INDEX

Exhibit No.	Description
99.1	Press Release issued by PDF Solutions, Inc. dated October 6, 2004.
99.2	Press Release issued by PDF Solutions, Inc. dated October 6, 2004.

EXHIBIT 99.1

News Release

FOR IMMEDIATE RELEASE

Corporate Communications Contact:
Jen Bernier
Armstrong Kendall, Inc.
408-997-7762
jen@akipr.com

Investor Relations Coordinator:
Sonia Segovia
PDF Solutions, Inc.
408-938-6491
sonia.segovia@pdf.com

PDF Solutions® and Chartered Team to Enable
Fast 90-Nanometer Process Ramp
PDF's Unique Characterization Vehicle® Methodology a
Key Factor in Leading Foundry's Selection

SAN JOSE, Calif., October 6, 2004 — PDF Solutions, Inc. (Nasdaq: PDFS), the leading provider of semiconductor process-design integration technologies and services, has announced that Chartered Semiconductor Manufacturing (Nasdaq: CHRT and SGX-ST: Chartered), one of the world's top three dedicated semiconductor foundries, is implementing the company's Integrated Yield Ramp (IYR) and Characterization Vehicle (CV™) Infrastructure at Chartered's 300-millimeter (mm) Fab 7 to expedite process ramp of 90-nanometer (nm) silicon-on-insulator and bulk CMOS technologies simultaneously.

"Our customers need world-class yields to be competitive in today's cost-driven environment," said Kay Chai "KC" Ang, senior vice president of fab operations at Chartered. "We have automated our 300-mm fab, which incorporates PDF Solutions' IYR methodology for resolving process margin, with a focus on meeting customers' manufacturability metrics and supporting process ramp in the fastest possible time."

"Our IYR solutions, including our CV Infrastructure, deliver yield and performance improvements at any stage of a process life cycle, from process development to maturity," said John Kibarian, president and CEO of PDF Solutions. "For Chartered's customers, this means higher initial yields, faster yield ramps, and higher mature yields. The result is cost-effective, high-volume production in less time."

PDF Solutions' IYR infrastructure combines patented methodology and technology with cross-functional service teams to deliver yield, performance, and reliability improvements to any stage of integrated circuit manufacturing. The CV Infrastructure includes CV test chips and pdFasTest™ hardware coupled with pdCV™ software, which enable fast isolation and repair of systematic and random physical mechanisms that limit process capability and yield.

About PDF Solutions

PDF Solutions, Inc. (Nasdaq: PDFS) is the leading provider of process-design integration technologies to enhance IC manufacturability. PDF Solutions' software, methodologies, and services enable semiconductor companies to create IC designs that are more manufacturable, and manufacturing processes that are more capable. By simulating nanometer-scale product and process interactions, PDF Solutions offers customers faster time-to-market, increased IC yield and performance, and improved product reliability and profitability. Headquartered in San Jose, Calif., PDF Solutions operates worldwide. For more information, visit www.pdf.com.

—end—

EXHIBIT 99.2

News Release

FOR IMMEDIATE RELEASE

Contacts:

PDF Corporate Communications:
Jen Bernier
Armstrong Kendall, Inc.
408-997-7762
jen@akipr.com

PDF Investor Relations:
Sonia Segovia
PDF Solutions, Inc.
408-938-6491
sonia.segovia@pdf.com

Virage Logic:
Sabina Burns
Virage Logic Corp.
510-743-8115
sabina.burns@viragelogic.com

PDF Solutions® and Virage Logic Partner to Create
Process-Aware Semiconductor IP Libraries
Creation of pDfx-Compliant Libraries Helps Designers Create Better Yielding ICs

SAN JOSE, Calif., October 6, 2004 — PDF Solutions, Inc. (Nasdaq: PDFS), the leading provider of semiconductor process-design integration technologies and services, and Virage Logic Corp. (Nasdaq: VIRL), a leading provider of semiconductor IP platforms, announced that the companies are partnering to develop process-aware extensions to Virage Logic's Area, Speed and Power (ASAP) Logic™ standard cell IP libraries. Through this collaboration, the Virage Logic libraries will be extended with DFM variants that incorporate PDF Solutions' learning from more than 25 yield ramps and yield simulation technology. The extended ASAP Logic libraries will be compliant with PDF Solutions' revolutionary pDfx process-aware design for manufacturability (DFM) environment, which integrates seamlessly with industry leading design flows to help designers create integrated circuit (IC) designs that are more manufacturable.

"Virage Logic is committed to helping its customers with their yield and manufacturability challenges and has a proven track record of providing memory yield improvements of up to 250% to its STAR Memory System customers," said Adam Kablanian, president and CEO, Virage Logic. "With access to PDF Solutions' pDfx, we will be able to offer advanced DFM capabilities throughout our semiconductor IP platform product portfolio, extending our ability to deliver on our commitment to providing customers with the IP necessary to successfully manage nanometer technology challenges."

"It will take cooperation between companies throughout the design and manufacturing chain to provide designers the tools they need to solve the increasing challenges associated with semiconductor yield," said John Kibarian, president and CEO, PDF Solutions. "We are very pleased to work with Virage Logic to add this important part of the pDfx infrastructure, which is designed to help Virage Logic's customers increase their profitability by creating better yielding designs. This alliance continues the industry's adoption of pDfx technology."

About the pDfx Process Aware Design Environment

The pDfx environment packages PDF Solutions' extensive knowledge of leading-edge IC manufacturability and delivers it directly to IC designers through the leading commercial synthesis and place and route EDA packages. Using pDfx, designers can optimize products for manufacturability before tapeout, which is designed to result in product cost savings and faster ramps to production-level yields. This reduces the need to re-spin mask sets for manufacturability issues, which is essential to designers as IC designs move to 130 nanometer and smaller technologies. pDfx is designed to integrate with proprietary and commercial intellectual property for the target process. pDfx is integrated in Magma's Blast Fusion and interoperable with Physical Compiler from Synopsys and First Encounter Global Physical Synthesis from Cadence. Initial design efforts using the pDfx environment have resulted in customers achieving yield improvements ranging from five- to ten-percent increases in net good die. This level of yield improvement gives customers of pDfx a major competitive advantage.

About Virage Logic's ASAP Logic and STAR Memory System

The ASAP Logic product line, based on Virage Logic's proprietary and patented routing methodology and cell architecture, contains application-optimized libraries targeted to unique market requirements. The ASAP Logic Standard Cell Libraries are optimized for area, speed, and power and provide up to a 30% increase in utilization when compared to conventional standard cell libraries.

The STAR Memory System provides the most integrated solution for the cost effective embedding, on-chip testing and repairing of multi-megabit memories. The system includes High-Speed, High-Density or Ultra-Low-Power memories to address a broad range of SoC design requirements. The system consists of one or more STAR and/or ASAP SRAM or ROM Memory blocks, a STAR Processor, a STAR JPC that provides a chip-level infrastructure hub to connect multiple STAR Memory System instances, a STAR Fuse Box and a STAR Builder to automate

the insertion of the STAR Memory System into the functional hierarchy of the design. With customers experiencing yield improvements of up to 250%, the STAR Memory System can potentially save millions of dollars in recovered silicon, substantially reduce test costs, and achieve shorter time-to-volume.

About PDF Solutions

PDF Solutions, Inc. (Nasdaq: PDFS) is the leading provider of process-design integration technologies to enhance IC manufacturability. PDF Solutions' software, methodologies, and services enable semiconductor companies to create IC designs that are more manufacturable, and manufacturing processes that are more capable. By simulating nanometer-scale product and process interactions, PDF Solutions offers customers faster time-to-market, increased IC yield and performance, and improved product reliability and profitability. Headquartered in San Jose, Calif., PDF Solutions operates worldwide. For more information, visit www.pdf.com.

About Virage Logic Corporation

Founded in 1996, Virage Logic Corporation quickly established itself as a technology and market leader in providing advanced embedded memory intellectual property (IP) for the design of complex integrated circuits. Virage Logic has evolved to become a global leader in semiconductor IP platforms comprising embedded memory, standard cells, and I/Os primarily for the consumer, communications and networking, handheld and portable, and computer and graphics markets. Virage Logic's highly differentiated product portfolio provides foundries, integrated device manufacturers (IDMs), and fabless customers with key competitive advantages including higher performance, lower power, higher density and optimal yield. The company's comprehensive quality efforts are validated in its FirstPass-Silicon Characterization lab, which ensures high quality, reliable IP across a wide range of foundries and process technologies. Headquartered in Fremont, California, Virage Logic has R&D, sales and support offices worldwide. For more information, visit www.viragelogic.com.

—end—

Forward-Looking Statements
The statements in this press release regarding pDfx and customer yield improvement are forward looking. Actual results could differ materially from those expressed in these forward-looking statements. Risks and uncertainties that could cause results to differ materially include risks associated with: any unforeseen industry changes; difficulties in modifying PDF's solutions on a timely basis; and changes in the marketplace for PDF's solutions, including the introduction of products or services competitive with PDF's products and services. Readers should also refer to the risk disclosures set forth in PDF's periodic public filings with the Securities and Exchange Commission, including, without limitation, its annual report on Form 10-K, most recently filed on March 15, 2004 (as amended), and its quarterly reports on
Form 10-Q, most recently filed on August 9, 2004. The forward-looking statements contained in this release are made as of the date hereof, and PDF does not assume any obligation to update such statements nor the reasons why actual results could differ materially from those projected in such statements.

SAFE HARBOR STATEMENT FOR VIRAGE LOGIC UNDER THE PRIVATE SECURITIES LITIGATION REFORM ACT OF 1995:
Statements made in this press release, other than statements of historical fact, are forward-looking statements, including, for example, statements relating to trends, business outlook, products, and customer relationships. Forward-looking statements are subject to a number of known and unknown risks and uncertainties, which might cause actual results to differ materially from those expressed or implied by such statements. These risks and uncertainties include Virage Logic's ability to forecast its business, including its revenue, income and order flow outlook; Virage Logic's ability to execute on its strategy to become a provider of semiconductor IP platforms; Virage Logic's ability to continue to develop new products and maintain and develop new relationships with third-party foundries and integrated device manufacturers; adoption of Virage Logic's technologies by semiconductor companies and increases or fluctuations in the demand for their products; the company's ability to overcome the challenges associated with establishing licensing relationships with semiconductor companies; the company's ability to obtain royalty revenues from customers in addition to license fees, to receive accurate information necessary for calculating royalty revenues and to collect royalty revenues from customers; business and economic conditions generally and in the semiconductor industry in particular; competition in the market for semiconductor IP platforms; and other risks including those described in the company's Annual Report on Form 10-K for the period ended September 30, 2003, and in Virage Logic's other periodic reports filed with the SEC, all of which are available from Virage Logic's website (www.viragelogic.com) or from the SEC's website (www.sec.gov), and in news releases and other communications. Virage Logic disclaims any intention or duty to update any forward-looking statements made in this news release.